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TEST STRUCTURE TO MICROCIRCUIT CORRELATION

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13. ABSTRACT *(Maximum 200 words)*

This Parametric Analysis of Radiation effects software development is given the general title PARA. This report describes the development of algorithms and source codes for the simulation of radiation effects on CMOS ICs. The project concentrated on the simulation of total dose effects and the ways to establish/predict the operational lifetime and radiation tolerance of ICs. The PARA switch level simulator incorporates the capability to assign bias dependent postirradiation drive parameters to transistors within a microcircuit and to calculate propagation delays based on those parameters. This permits test vectors to be assigned based on worst case postirradiation propagation delays.

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1.0 INTRODUCTION

Demonstration of radiation hardness of microcircuits has relied on destructive radiation testing of the product (Qualified Parts List, QPL). Recently, controlling the manufacturing process steps which affect radiation hardness has been initiated. The QML (Qualified Manufacturers List) approach is to "process in" the radiation hardness. Statistical Process Control (SPC) is an integral part of the QML methodology. Implementation of SPC for total dose hardness assurance requires identification of relevant process and device parameters. A correlation must be established between the response of microcircuits and test structures fabricated on the same process line. The final step is the control of device parameters through the control of process steps during fabrication. Device parameters can be measured on each wafer from test structures placed on a drop-in process monitor or in the kerf between microcircuit die. The key to establishing the correlation of device parameters and microcircuit response is the development of accurate microcircuit simulators (Refs. 1 and 2). Results from the microcircuit simulations can be used to determine the SPC for active and parasitic circuit parameters which is necessary to assure total dose hardness of the microcircuit.

The purpose of this study was to identify circuit parasitics and device parameters which affect the ionizing radiation degradation of microcircuit performance. The test vehicle for this program was the Honeywell Yield and Circuit Reliability Analysis Test chip (YCRAT). This test chip contains test structures for the extraction of circuit parasitic and device parameters, and microcircuits to determine correlations between the parameters and microcircuit response. Work on this program was conducted by Mission Research Corporation (MRC) and Sandia National Laboratory (SNL). Mission Research was responsible for extracting SPICE models and the corresponding parameters for microcircuit simulation. Sandia was responsible for the development of a wafer level test capability.

2.0 BACKGROUND

There are two principle modes by which CMOS microcircuits can fail in an ionizing environment: (a) power supply current, and (b) timing. Power supply current can increase due to leakage between adjacent transistors or an increase in the drain-to-source current of n-channel transistors in the off condition. Timing changes occur from threshold voltage shifts and mobility degradation in the n- and p-channel transistors. For the p-channel transistor, the effects of oxide trapped charge and interface traps are additive, and the threshold voltage shift is always negative. This reduces the drive capability of the p-channel transistor. For the n-channel transistor, oxide trapped charge effects move the threshold voltage toward depletion mode operation while interface states cause a shift toward enhancement mode. Depending on the direction of the threshold voltage shift, and the portion of the shift due to interface traps, the drive capabilities of the n-channel transistors can increase or decrease. The drive capability of the transistors determine the time necessary to charge or discharge a circuit node.

Simulation of changes in circuit timing requires the inclusion of circuit parasitic resistors and capacitors. These parasitic elements combined with the drive capability of the transistor determine charge and discharge time of internal microcircuit nodes, and can be located at the transistor (i.e., contact resistances, gate overlap and junction capacitances, etc.) or at the interconnects between the transistors (i.e., polysilicon resistance, interdielectric capacitances, etc.). The location and a unit of measure of parasitic elements can be determined by examination of the circuit layout. Values per unit of measure of the parasitic elements can be obtained through measurement of test structures.

To identify the transistor and parasitic circuit parameters which affect the microcircuit radiation hardness (which must be brought under SPC), there must be a demonstration of the capability to map pre- and postirradiation test structure parameters into

predictions of pre- and postirradiation responses of the microcircuit. This mapping can be performed using SPICE circuit simulation tools. However, the complete microcircuit function usually cannot be simulated because of the number of circuit elements in VLSI technologies. To reduce the number of circuit elements, simulation of a critical path through the microcircuit is used.

3.0 APPROACH

The Honeywell YCRAT test chip, fabricated with the RICMOS 3, P substrate/N well, technology, is an excellent test vehicle for studying the capability of modeling total-dose induced changes in circuit timing. The total-dose induced increase in circuit timing can be modeled for a delay chain and a **16k** SRAM. Test structures located on the same die can be used to determine the changes in transistor parameters as a function of total dose and for determining the parameters of the circuit parasitic elements. The RICMOS 3 process uses a hardened field oxide technology which has been shown to prevent transistor-to-transistor and transistor edge leakage paths. All necessary test structures for determination of circuit parasitics and MOS transistor parameters are on the same die with a 50-inverter delay chain and a 2k x 8 SRAM. Fifty-two YCRAT die are on each wafer. The delay chain was designed so that the input signal is propagated through the 50 inverters for a high-to-low input pulse. A low-to-high input pulse measures only the instrumentation, and input and output buffer delay. However, the delay attributed to the 50 inverters cannot be directly calculated by subtracting the rise and fall time delays, because of the nonsymetric delays in the input and output buffers and test instrumentation.

Most work station software supports the creation of SPICE netlists (a description of how the elements of a circuit are interconnected) from GDS II layout tapes. Circuit elements are recognized through logic manipulation of the mask levels of the technology. The work station software also generates the appropriate areas and perimeters of the circuit elements. For example, calculations for the transistor include: (a) gate length and width, (b) area of the source and drain, and (c) perimeter of the source and drain. For gate interconnect polysilicon resistance and capacitance to the substrate, the number of squares and the area are calculated.

The parameters for SPICE models were derived using measurements from test structures which are at the same die location as the modeled microcircuit. The transistor DC

parameters were determined using MOSFIT, an in-house parameter extraction program. This program uses a curve fit procedure which minimizes the error between the data and SPICE MOSFET p- and n-channel models. The parasitic transistor parameters were calculated from test structure data and process information. These parameters include (1) source and drain junction capacitance, (2) gate capacitance, and (3) source and drain overlap (miller) capacitances. The reduction in channel length and width was calculated from transistors of different lengths and widths. The parameters for parasitic circuit resistors and capacitors came from test structure data or process information with the appropriate area or perimeter correction.

A SPICE model was developed for the delay chain. SPICE model predictions were performed by using test structure data from a given die location to generate die-location-specific SPICE model parameters. The SPICE model was verified on a three die locations. The goal was to generate a SPICE model for the delay chain which would be accurate to within +/- 5 percent for pre- and postirradiation data at those die locations. After verification, the model will be applied to other die sites using up to three wafers to quantify the accuracy of the model. The goal is to identify the model parameters which correlate to the total dose response of the delay chain.

4.0 WAFER LEVEL TESTING

The wafer-level test system at SNL is a 10 keV ARACOR x-ray irradiator (including a wafer prober) interfaced to an HP4062 parametric tester for test structure measurements, and to an HP82000 (50 MHz) tester for parametric and functional IC measurements. The tester, coax cables, and probe card had a matching 100 ohm impedance. The ARACOR and the two test systems are controlled by an HP375 workstation. A complete description of the radiation and test capability is given in Reference 3.

Sandia supported MRC in the modeling effort by providing test structure and microcircuit data. Mission Research and SNL together defined the pre- and postirradiation test procedures for each die.

Prior to irradiation, test structures were measured to determine:

- The circuit parasitic resistor and capacitor parameters,
- The parasitic MOSFET model parameters and effective channel length and width.

Pre- and postirradiation measurements included:

- The test structures for DC MOSFET model parameters.
- The delay chain timing measurement.

Delay chain measurements were made using both a high-to-low input pulse to measure the delay combination of the 50 inverters and the input output buffers, and a low-to-high input pulse which only measures the delay associated with the buffers. The HP82000 was set to accept a low-to-high transition when the output buffer voltage was 2.5 V or greater. The high-to-low output buffer transition voltage was set at 2.4 V.

The delay chain and MOSFET test structures were measured in the ARACOR irradiator preirradiation and postirradiation starting at 10 krad (SiO_2) following a 1, 3, 5 increment

up to 1 Mrad (SiO_2). Thereafter, measurements were performed at each 1 Mrad (SiO_2) increment to a maximum dose of 5 Mrad (SiO_2). Anneal data were recorded for 15 minutes. Each delay chain measurement was performed at three supply voltages, 4.5, 5.0, and 5.5 V. A description of the individual test structures used in pre- and postirradiation measurements is provided in the modeling section, which discusses the incorporation of the data into the microcircuit model.

5.0 MODELING

During this phase of the test structure to microcircuit correlation study, work was conducted primarily in three areas. First, computer automated capabilities were developed using DRACULA workstation software to extract a SPICE netlist for the delay chain from the RICMOS YCRAT GDS-II layout tape. Second, data from test structures had to be reduced to derive parameters for the delay chain microcircuit model. Test structure data were incorporated into the SPICE netlist extraction routine to derive the parasitic circuit elements parameters. The device model parameters were derived using MOSFET test structure data and the curve fitting program MOSFIT. Finally, delay chain simulations were performed and compared to measured data. Each area of this study will be described in greater detail.

5.1 SPICE NETLISTS

Extracting a SPICE netlist for a microcircuit from GDS-II layout information involves identifying circuit elements which include NMOS and PMOS transistors, resistors, and capacitors. Identification is performed by symbolic logic representation of the mask layers. All circuit elements are defined by using mask layers and logic operators (i.e., AND, OR, and NOT). The area(s) and perimeter(s) for each circuit element are calculated as required for parameterization. For instance, a metal 1 to metal 2 capacitor is defined by ANDing the metal 1 and metal 2 masks. The area of the intersection is calculated and used to define the value of the capacitor. The symbolic logic representations of the circuit elements are included in a technology file. This information can be used to extract SPICE netlists for any circuit in RICMOS 3 bulk technology.

The technology file required for this modeling effort contained substantially more information than is included in a standard technology file. Generally, the technology file is used to only identify intentional circuit elements for layout versus circuit schematic

checks, and layout spacings in design rule checks. Significant effort was required to extend the capabilities to create a standard technology file to include identifying circuit parasitics and calculating the area, perimeter, and number of squares as required for the circuit parasitic. Circuit parasitic resistors arise from metal, polysilicon, and silicon resistivity, and the resistance of vias and contacts. Circuit parasitics capacitances arise from interdielectric separation of metal, polysilicon, and silicon, and from silicon junctions. The calculation of the unit measure for some of the MOSFET parameters was complicated by sharing of the areas; for instance, two NMOS transistors sharing a common source. The capability to extract the parasitic and device elements and its unit of measure was verified using visual checks of the layout on the work station.

SPICE netlists were generated for each die location by using data from test structures on that die location. Data from the test structures were converted into the resistance or capacitance per unit of measure (e.g., area). These values were input into the technology file. The value of each circuit element in the SPICE netlist was calculated by multiplying the size of the element in the unit of measure times the parameter value per unit of measure. For example, the resistance of a polysilicon gate interconnect was calculated by: (a) extracting the number of squares from the layout, and (b) calculating an ohm per square value from a test structure. During software generation of the SPICE netlist, all polysilicon resistors in squares were multiplied by the ohm per square parameter value. This information together with MOSFET model parameters was used to generate die specific SPICE netlists.

All microcircuit simulations were run on PSPICE. This member of the SPICE family of circuit simulators was chosen for two reasons. PSPICE is continually updated, and can be run with consistent outputs on multiple computer platforms. Mission Research has both DEC and SUN workstations as well as 386 and 486 PCs.

SPICE netlists were generated for the delay chain. The pre- and postirradiation predictions of the delay chain propagation times were compared to the measured value. A preliminary goal of a prediction accuracy of +/- 5 percent was set for pre- and postirradiation measurements at each die location. The SPICE netlist extraction routine was examined for errors or oversights. The required accuracy was verified at three die locations.

5.2 PARAMETER EXTRACTION

The parameters required to define a die specific microcircuit model can be divided into two distinct sets: (a) the parameters for the circuit parasitics identified through the technology file, and (b) the MOSFET model parameters. Values of these parameters are determined using test structures on the same YCRAT die location as the microcircuit and/or process information supplied by Honeywell. The method for determining a given parameter was defined by analyzing the test structure and the capability of wafer level measurement. The first choice was always to measure a test structure. This approach provides information on actual parameter distributions on the measured wafers and the effect on the microcircuit response. However, some test structures were found to be inappropriate for wafer level measurement. Specific details for each circuit parasitic and MOSFET parameters are discussed below.

5.2.1 Circuit Parasitics

Circuit parasitics identified through the technology file include interdielectric capacitors, metal and polysilicon interconnect resistances, and contact and via resistances. Table 1 lists these circuit parasitics and the method of parameter extraction, which includes the type of test structure and the unit of measure. If process information was used to derive parameters for the circuit element, it is listed under the test structure column. The unit of measure refers to the calculated size of the resistor or capacitor during the extraction of the circuit element from the layout.

Table 1. Circuit parasitics.

CIRCUIT PARASITICS	TEST STRUCTURE	UNIT OF MEASURE
Interdielectric Capacitors		
Metal 1 to Poly	process information	area
Metal 1 to Well	process information	area
Metal 1 to Sub	process information	area
Metal 1 to Metal 2	process information	area
Poly to Well	process information	area
Poly to Sub	process information	area
Contact and Via Resistance		
Metal 1 to P^+	kelvin	perimeter
Metal 1 to N^+	kelvin	perimeter
Metal 1 to Poly	kelvin	perimeter
Metal 1 to Metal 2	kelvin	perimeter
Resistors		
Gate Interconnect Poly	crossbridge	ohm/sq
High Rho Poly	Van Der Pauw	ohm/sq
Metal 1	crossbridge	ohm/sq
Metal 2	crossbridge	ohm/sq
P^+	crossbridge	ohm/sq
N^+	crossbridge	ohm/sq
LDD	Van Der Pauw	ohm/sq

The test structures for calculating circuit parasitics resistors and capacitors, were measured during preirradiation only. These circuit parasitics should not be sensitive to ionizing radiation.

All interdielectric capacitors were determined from Honeywell process information. Test structures were available for these measurements, but the capacitances of these structures are < 5 pf. To accurately measure a sample distribution, a test system capability of at least 0.5 pf would be required, which is impractical for a wafer probe. Thus for interdielectric capacitors, process information was used instead of measured

data in which sample to sample variation would be dominated by measurement system noise. The process information for each interdielectric capacitor is in farads per area, so the area of these interdielectric capacitors was extracted from the layout.

Test structures were used to determine the resistor parameters. The resistance of the polysilicon and metal interconnects were calculated using the standard ohm per square approach. However, the perimeter was used instead of the area for the contact and via resistors. Previous analyses of current densities in vias and contacts using BUSNET (power bus design and analysis work station software tool) suggest the current density is much larger at the perimeter of the contact than in the center. Since most of the current is near the perimeter, the resistance of the contact or via is closer to being a function of the perimeter than of the area.

5.2.2 MOSFET Model Parameters

The NMOS and PMOS model parameters are dependent on the PSPICE MOSFET device model. The MOSFET model has different levels which refer to the different models. Level 3, a semi-empirical, short-channel model, was used in the microcircuit simulations. The level 3 MOSFET model parameters can be separated into three categories: (a) the parameters which define the size of the transistor and are extracted from the layout, (b) parameters which define the DC characteristics, and (c) the parasitic leakage and capacitance parameters.

The parameters which defined the size of the MOSFET were extracted from the layout. These parameters include the as-drawn channel length (L) and width (W), and the areas and perimeters of the source (AS, PS) and drain (AD, PD). The dimensions of the source and drain are used by PSPICE in the calculation of the junction capacitances.

The MOSFET level 3 DC model parameters are given in Table 2. These parameters define the inversion characteristics of PMOS and NMOS transistors. The goal was to set

the parameters for the model to achieve the best possible agreement between actual and simulated MOSFET inversion characteristics. Some NMOS and PMOS transistors of various lengths and widths were measured to define the DC model parameters. Each MOSFET was measured at multiple gate and drain potentials. First, the gate voltage was incremented from 1 to 5 V in steps of 1 V. At each gate voltage, the drain voltage was swept from -1 to 5 V. (The gate and drain voltage are opposite in sign for p-channels.) This measurement established the drain curves for the MOSFET. A second measurement was performed with the drain voltage at 0.15 V and the gate was swept from -1 to 5 V. This measured the subthreshold and linear inversion characteristics of the MOSFET.

Table 2. MOSFET Level 3 DC model parameters.

PARAMETER		
NAME	DEFINITION	PARAMETERIZATION
L	as-drawn channel length	GDSII layout
W	as-drawn channel width	GDSII layout
LD	lateral diffusion-length	test structure
WD	lateral diffusion-width	test structure
TOX	oxide thickness	test structure
XJ	metallurgical junction depth	process information
NSUB	surface doping density	process information
VTO	zero-bias threshold voltage	MOSFIT
PHI	surface potential	MOSFIT
UO	surface mobility	MOSFIT
VMAX	maximum drift velocity	MOSFIT
THETA	mobility modulation	MOSFIT
ETA	static feedback	MOSFIT
KAPPA	saturation field factor	MOSFIT
GAMMA	bulk threshold parameter	MOSFIT

Eight of the DC model parameters in Table 2 were determined using a curve fitting program called MOSFIT. This program uses the channel length (L), width (W), lateral diffusions (LD, WD), the oxide thickness (TOX), the source and drain junction depths (XJ), and the surface doping concentration (NSUB) as input. These parameters are held constant during the fitting procedure. The remaining parameters are allowed to vary to achieve the best fit to the measured data. A procedure was established to achieve the best fit and maintain the physical meaning of the model parameters. A set of typical starting values was given to the eight MOSFIT parameters used in the fitting procedure. The first fit was performed allowing VTO, PHI, and U to vary while holding the remaining parameters fixed. A second fit was performed allowing all eight parameters to vary.

The values of the seven parameters (L, W, LD, etc.) which were held constant throughout the MOSFIT procedure were not critical to achieving a good fit to the DC characteristics. (MOSFIT would adjust the varied parameters to achieve a good fit.) However, these parameters did have a direct impact on the AC performance of the modeled MOSFET. Therefore, it was necessary to obtain accurate values for these parameters. The parameters L and W were obtained from the layout. The parameters NSUB and XJ were taken from process information, since no test structures exist for accurate empirical measurement. The parameter TOX was obtained from polysilicon gate oxide capacitors over the substrate for the n-channel, and over the well for the p-channel. The lateral diffusions WD and LD were used to determine the effective channel length and width of the MOSFET. The technique used for the calculation of WD is given in Reference 4. This technique requires measurements to be taken on multiple MOSFETs with fixed length and various widths. Data taken at a drain voltage of 0.15 V from 50/1.2 and 3.5/1.2 (width/length) dimension MOSFETs were used in the calculation. Two techniques were applied for the calculation of LD. This measurement is complicated by the use of an LDD structure in the RICMOS 3 technology. Both techniques were applied using three transistor dimensions, 10/10, 10/1.5, and 10/1.2. The curve fitting procedures for the calculation of LD in Reference 5 yielded poor

correlations. This caused a large uncertainty in the LD calculation. The technique in Reference 6 had an acceptable curve fit for the LD calculation. However, the calculated LD is negative for the n-channels. Reference 6 suggests this may be due to the LDD diffusion. The determination of LD used in the delay chain simulations is discussed in Section 5.3.

The MOSFET model junction and capacitance parameters are given in Table 3. These parameters affect the AC performance of the MOSFET. The source/drain to substrate (well) junction leakage per unit area (JS) was taken from process information. PSPICE uses the areas of the source and drain times JS to determine the leakage for each junction. The bottom and sidewall junction capacitances were calculated using two test structures. The two structures had different area (bottom) to perimeter (sidewall) ratios. If it was assumed that the sidewall and bottom capacitances are additive, the data from the two structures were solved simultaneously to calculate the contribution of the capacitance per unit area (CJ) and the capacitance per unit perimeter (CJSW) separately. PSPICE uses the areas and perimeters of th source and drain together with CJ and CJSW to scale the capacitance for each MOSFET. PSPICE uses the effective channel width (W-2WD) times the channel length (L-2LD) to calculate the capacitance associated with the MOSFET gate. The gate capacitance is divided between gate-to-drain, and gate-to-source depending on the MOSFET operating condition.

Table 3. MOSFET Level 3 parasitic parameters.

PARAMETER		
NAME	DEFINITION	PARAMETERIZATION
JS	bulk p-n saturation current/area	process information
PB	bulk p-n bottom potential	test structure
MK	bulk p-n bottom grading coefficient	test structure
CJ	bulk p-n zero-bias bottom cap/area	test structure
PBSW	bulk p-n sidewall potential	test structure
MJSW	bulk p-n sidewall grading coefficient	test structure
CJSW	bulk p-n zero-bias sidewall cap/area	test structure

Values for the MOSFET models had to be determined pre- and postirradiation. Most of the parameters are not affected by ionizing radiation. The only parameters assumed to change as a result of ionizing radiation were the parameters in Table 2 that were derived using MOSFIT. Before irradiation, these parameters were derived using data from 10/1.2 n- and p-channel transistors. Since the degradation of MOS transistor characteristics are a strong function of the gate bias during irradiation, irradiations were performed with the transistors in both the on and off conditions. On the same die location, 50/1.2 n- and p-channel transistors were held off during irradiation and 10/1.2 n- and p-channel transistors were held on during irradiation. These four transistors were used to define the postirradiation MOSFET models for p-channel on and off, and n-channel on and off conditions.

5.3 DELAY CHAIN MODELING

A SPICE model for the delay chain needs to consider all aspects of parameter extraction and the HP82000 IC tester electrical and software characteristics. The delay chain SPICE model was extracted from the GDSII tape. Parameters for the circuit elements were extracted from test structures or process information as discussed in Section 5.2. However, two additional topics for MOSFET model parameter extraction need to be

discussed. First, the MOSFET model parameters were scaled to each transistor length and width variation in the delay chain to match both the DC and AC characteristics. Second, postirradiation modeling of the delay chain included the effects of circuit bias during irradiation. To compare SPICE model predictions and HP82000 measurements required: (1) the input and output waveforms to be modeled in SPICE, and (2) a similar electrical measurement approach.

Channel length and width parameters affect both the DC MOSFET characteristics, and the AC response which is dominated by the MOSFET gate capacitance. The delay chain and SRAM were designed with a constant as-drawn channel length of 1.2 μm. Only the channel width is varied depending on the circuit function. This allowed MOSFET DC model parameters to be scaled to the individual transistors in the delay chain only using channel width. The MOSFET test structure DC characteristics can be matched regardless of the effective channel length (L-2LD) used in the SPICE MOSFET model. This freed the effective channel length to be used to scale the gate oxide capacitance without influencing the DC characteristics. The area of the gate oxide capacitor is equal to the effective channel length times the width. A trial and error approach was used to optimize the effective channel length for all die locations at 1.1 μm. Variations in channel length from die to die were not used due to the measurement problems caused by the LDD diffusion.

The delay chain radiation response was measured as a function of total dose in the SNL ARACOR irradiator. Irradiation of the delay chain was performed in the static mode. This set the individual MOSFETs which compose the delay chain in either the on or off condition. The preirradiation delay chain model was constructed using the preirradiation n and p-channel MOSFETs models. The postirradiation delay chain circuit model was constructed differentiating between the MOSFETs which were on or off during irradiation. The P-ON and P-OFF, and N-ON and N-OFF MOSFET postirradiation models were combined with the delay chain circuit model to model the delay chain radiation response.

The delay chain SPICE model was constructed using 10 inverters and the input and output buffers. Only 10 inverters, instead of the 50 inverters in the actual delay chain, were included in the SPICE model to decrease the CPU time required to simulate the delay chain response. The simulated delay through the 10 inverters was used to calculate the delay that would have been simulated using 50 inverters. The delay through the middle 6 of the 10 inverters was extracted from the SPICE simulation. (The delay through the first and last 2 inverters can be influenced by the input and output buffers.) This delay was multiplied by 40/6 to calculate a delay for 40 inverters. The calculated 40 inverter delay was added to the simulated delay of 10 inverters and the input and output buffers, to arrive at a simulated delay chain response that could be compared to the measured radiation response on the ARACOR.

To achieve an accurate simulation of the input and output buffer delay, the pulse shape into and out of the delay chain was considered as well as the effects of the HP82000 calibration. The pulse shape into the delay chain input buffer is a function of the drive capability of the HP82000 IC tester, the transmission line between the tester and the delay chain probe card, and the probe card parasitics. The delay chain output buffer pulse shape is a function of the parasitics associated with the HP82000, the transmission line, and the probe card. Representations of the rise and fall characteristics of the input and output delay chain waveforms were determined using HP82000 tester specifications and delay chain measurements which bypassed the 50 inverters. A resistor, capacitor, and a linear pulse rise time were added to the SPICE model to create the specified input rise and fall pulse characteristics of the HP82000. The resistor and capacitor were used to add exponential pulse characteristics near ground and the positive supply voltage. The output waveform characteristics were modeled using a 100-ohm resistance to ground (matching the tester impedance) with additional resistor and capacitor components for the effects of the probe card. These components were determined through trial and error using the delay chain measurements at 4.5, 5.0, and 5.5 V.

Comparison of SPICE model predictions to actual delay measurements made on the HP82000 tester must consider propagation delays and the effects of the HP82000 calibration program. The SPICE model delays were measured from the start of the input rise or fall pulse to the output high-to-low transition at 2.4 V or the low-to-high transition at 2.5 V. The model output transition voltages matched the HP82000 output transition voltages. The HP82000 delay measurement was made in a similar approach. The HP82000 was calibrated for internal delays and the transmission line length. This calibration delay was subtracted by the HP82000 from every timing measurement. This calibration delay includes internal tester delays and signal propagation delays to the probe card. The comparison of measured and SPICE modeled delays were compared by choosing a single delay measurement (i.e., die location 3.3, preirradiation, 5.0 V power supply) for matching of the measured and modeled delays. This difference was subtracted from all the other SPICE modeled delays from other die locations and power supply voltages, pre- and postirradiation.

6.0 DELAY CHAIN MODEL RESULTS

Development of the ARACOR wafer level irradiation and test capability, and the pre and postirradiation modeling capabilities were performed concurrently. Test structure and delay chain data from three die locations on a single wafer were used to construct and verify the SPICE modeling procedures described in Section 5.0. The SPICE model was used to construct predictions for the delay chain irradiation response. These predictions were compared to measurements of the delay chain at the wafer level, preirradiation and at 5 Mrad (SiO_2).

The results for the three die locations are given in Table 4. The die locations indicators given in Table 4 refer to the row and column position of the die on the wafer. The SPICE model prediction and measured data were matched at die location 3.3, preirradiation, and 5.0 V supply voltage. The difference between the SPICE model prediction and measured data was 4.59 ns. Therefore, 4.59 ns were subtracted from each SPICE model delay prediction in Table 4. The model predictions for both die locations 3.3 and 3.6 match the measured data to < 1.5 percent error except die location 3.3, postirradiation at 4.5 V supply voltage. For die location 6.3 the error between the measured and model predictions increased to near 5.0 percent except again at the postirradiation and 4.5 V supply voltage. In summary, the largest errors between the PSPICE model predictions and the HP82000 measured data occurred at a supply voltage of 4.5 V and at die location 6.3.

Table 4. Comparison of the predicted and measured delay chain radiation response at 5 Mrad (SiO_2).

	Time (ns)			
Supply Voltage	Preirradiation		5 Mrad (SiO_2)	
	Measured	Model	Measured	Model
Die location 3.3				
4.5	55.3	55.52	63.0	60.67
5.0	48.9	48.90	53.1	53.20
5.5	44.4	44.45	47.8	48.43
Die location 3.6				
4.5	74.6	75.32	83.3	83.95
5.0	64.4	64.24	70.1	70.70
5.5	58.3	57.45	62.9	62.33
Die location 6.3				
4.5	55.1	53.60	63.0	57.59
5.0	48.6	47.76	53.0	50.58
5.5	44.4	42.92	47.7	45.70

7.0 DELAY CHAIN MODEL SENSITIVITIES

Analysis of the errors between the measured and modeled delay chain response showed two key features which could affect the predictive capability of the SPICE model. First, the increase in the measured delay from pre- to postirradiation at a supply voltage of 4.5 V for die locations 3.3 and 6.3 is a factor of 2 larger compared to the other supply voltages. The model predicted postirradiation delay does not agree with the larger increase in the postirradiation response at 4.5 V. Die location 3.6 did not show a factor of two increase at 4.5 V and there was good agreement between the modeled and measured response. Since the percent increase in measured postirradiation delay at 4.5 V supply voltage was not consistent across die locations, the input and output waveforms at the HP82000 were checked. Figure 1 is a diagram showing the procedures used for measuring the input and output waveforms. The output waveform should be measured at the input to the HP82000 for proper model comparison. However, the connections at the HP82000 did not provide any access for probes. Figure 2 shows the measured waveforms at the probe card of a HP82000 delay chain measurement. The input and output waveforms are shown in greater time detail in Figure 3. The input waveform to the delay chain has fall time characteristics which are in good agreement with the HP82000 specifications. The delay chain output buffer rise characteristics shows a ledge which persists for 20 ns at $\approx$ 2.5 V. This ledge is probably caused by a reflection in the transmission line between the probe card and the HP82000. This ledge occurs near the HP82000 programmed low-to-high transition voltage used for the measurements in Table 4. To verify that the ledge occurs at the HP82000, the low-to-high transition voltage was increased. At a low-to-high transition voltage of 3.0 V, the measured delay increased $\approx$ 20 ns. Opposite polarity waveforms shown in Figure 4 were measured which bypass the 50 inverters. The output waveform from the delay chain buffer shows a similar ledge. Based on the waveform analysis, the measured delays at 4.5 V for die locations 3.3 and 6.3 probably were affected by the distorted output waveform.

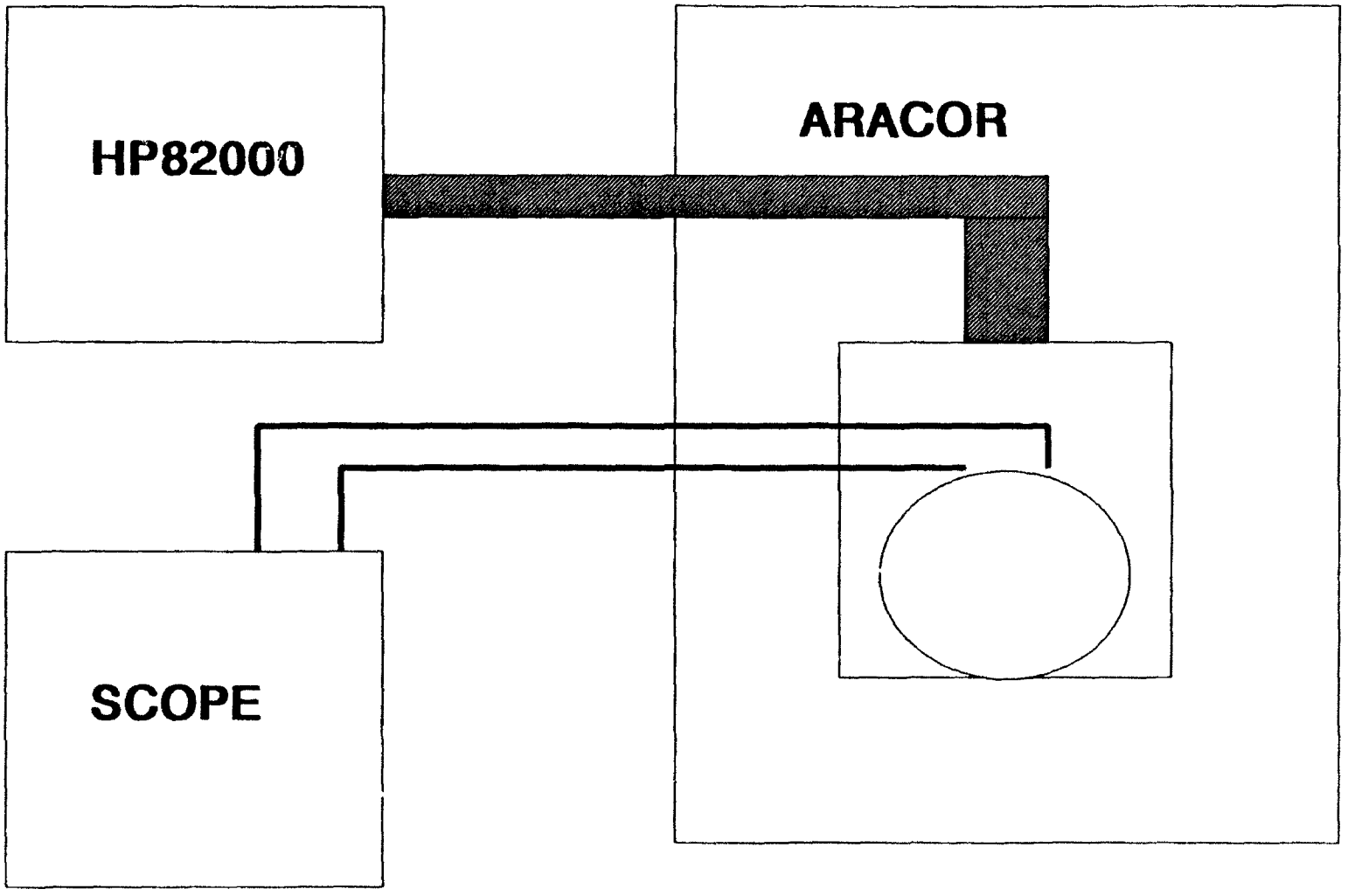


Figure 1. Location of input/output delay chain measurements.

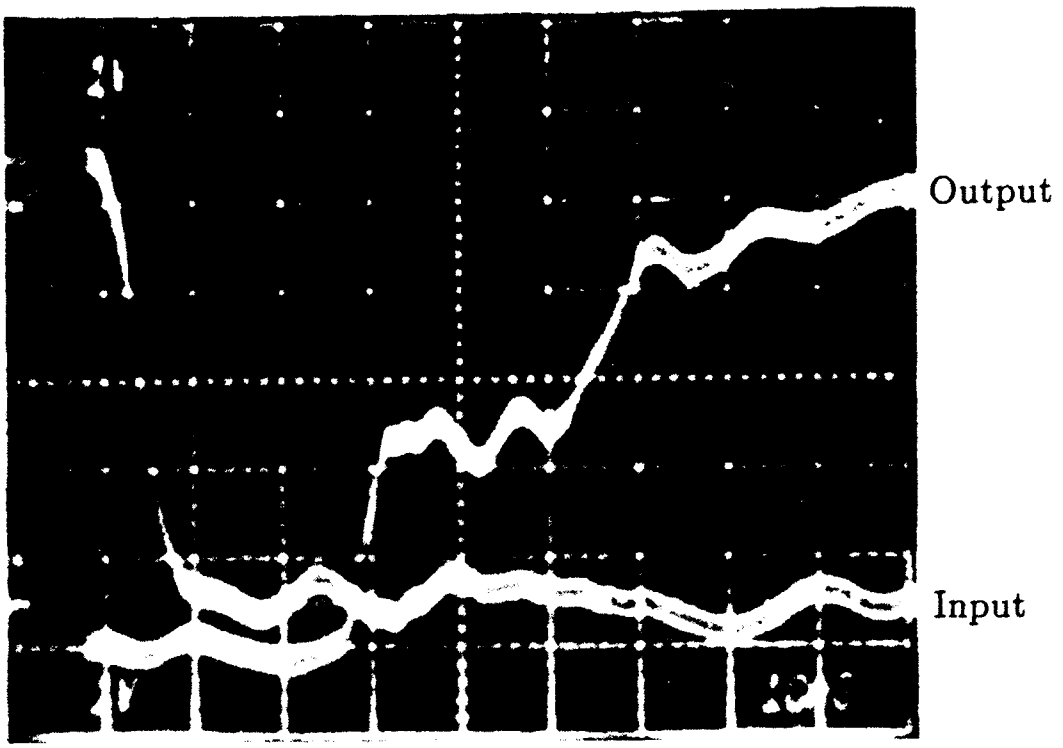
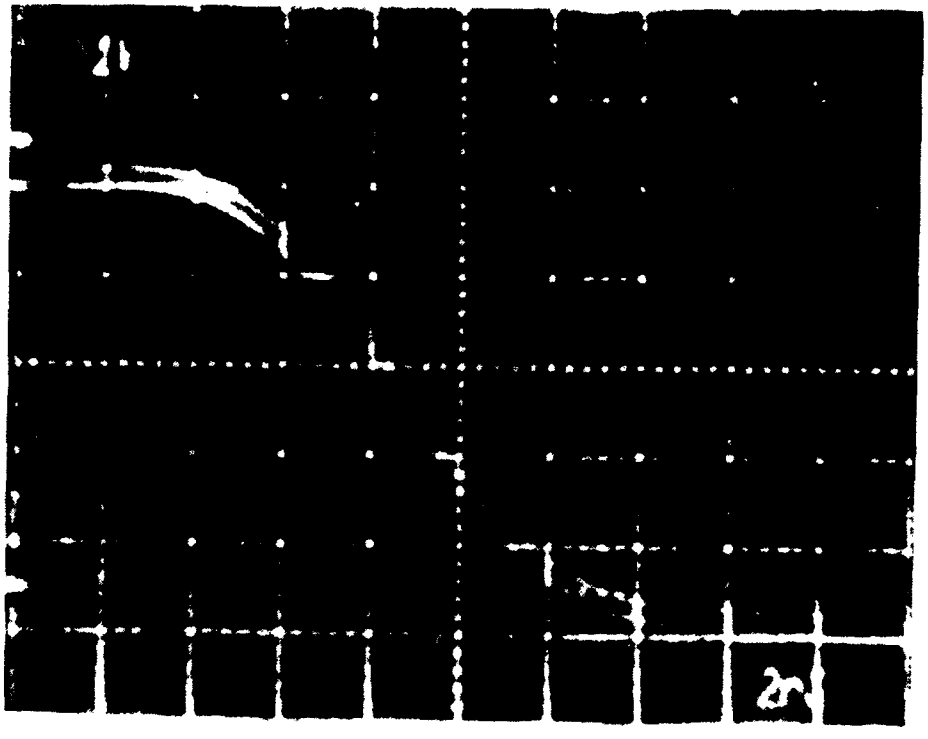
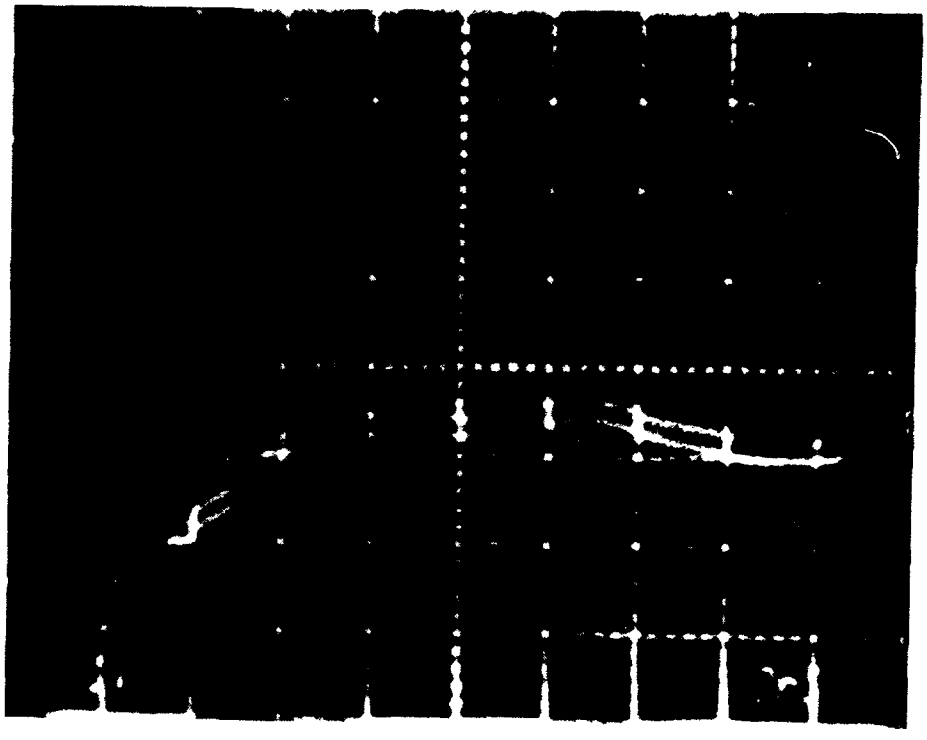


Figure 2. Delay chain waveform oscilloscope measurements at a 5.0 V supply voltage. The scales are 1.0 V and 10 ns per division.



(a) input waveform

Figure 3. Delay chain waveform measurement identical to Figure 2 except the scales are changed to 1.0 V and 2.0 ns per division.



(b) output waveform

Figure 3. Concluded.

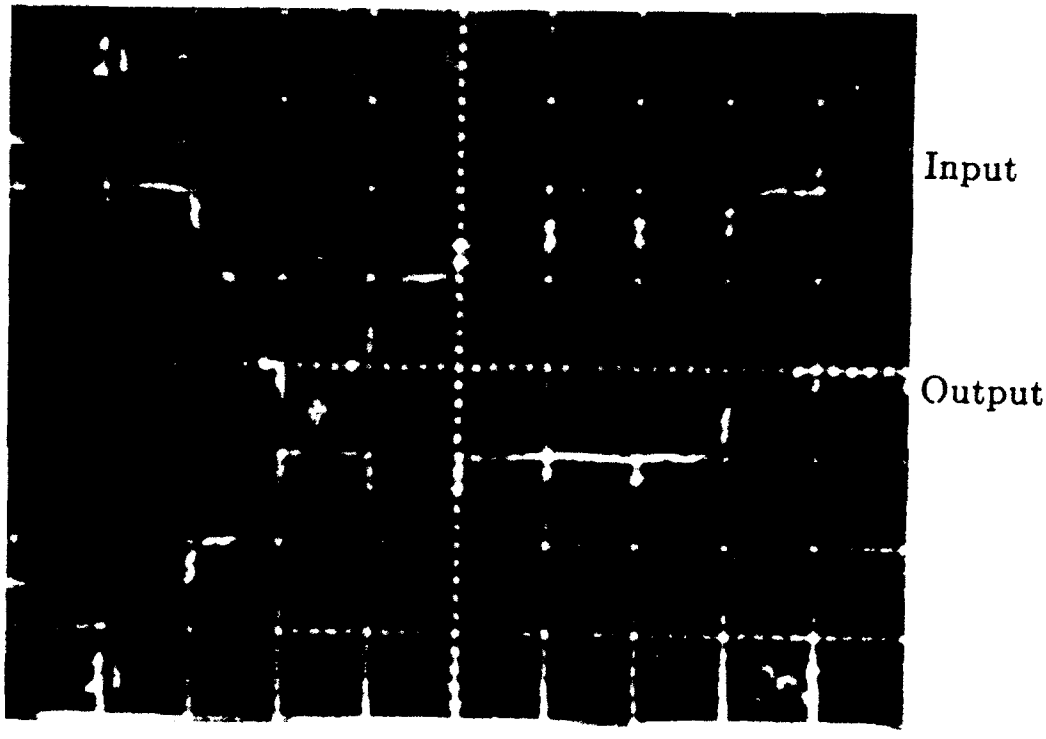


Figure 4. Delay chain waveform measurement bypassing the 50 inverters showing the delay due to input and output delay chain buffers. The supply voltage was at 5.0 V. The scales are 1.0 V and 2.0 ns per division.

For good agreement between the measured and modeled delays, the low-to-high transition voltage must occur at the 1 V per 2 ns output rise shown in Figure 3. To eliminate potential measurement problems, the low-to-high transition in the HP82000 was changed from 2.5 V to 1.5 V. Likewise, the high-to-low transition was changed from 2.4 V to 3.5 V for all future testing.

The second key feature which could affect the predictive capability of the SPICE model involves the differences in the modeled response of die locations 3.3 and 6.3. The HP82000 pre- and postirradiation delay measurements were very close for these two die locations. However, the model predicted less delay in die location 6.3. The faster response was traced to the DC characteristics of the n-channel MOSFET test structures. The current drive at a fixed MOSFET drain-to-source and gate-to-source voltages was larger at die location 6.3. This larger drive was not offset by any increase in the parasitic MOSFET gate capacitance. The effective channel width was similar for both die locations. The effective channel length was fixed at 1.1 μm for all die locations. The modeled increased drive at die location 6.3 may be a function of the polysilicon line width which determines gate length, and the LDD diffusion. A larger polysilicon line width may increase the drive of the n-channel MOSFET, but this would also increase the gate capacitance. The increase in gate capacitance would oppose the benefits of the increased drive.

To include the polysilicon linewidth in the determination of the effective channel length in future testing, the linewidth will be measured using a polysilicon crossbridge test structure. The polysilicon crossbridge was designed to have an as-drawn linewidth of 1.2 μm, equivalent to the MOSFET gate length of all transistors in the delay chain and SRAM. The variation in polysilicon linewidths from die to die will be included in the effective channel length. The difference at a given die location from the expected polysilicon linewidth for the technology will be subtracted from the nominal effective channel length of 1.1 μm. If required, the nominal effective channel length will be modified to center the SPICE modeled data to the measured data.

Using the SPICE model data given in Table 4, two changes were incorporated into the test structure and delay chain measurement procedures to be used in future pre- and postirradiation testing. The HP82000 low-to-high and high-to-low transition voltages were changed to eliminate potential measurement problems caused by poor delay chain output buffer rise and fall characteristics. Preirradiation measurement of a polysilicon crossbridge was added to extract the polysilicon linewidth. The die dependent linewidth will be used to scale the effective channel length which affects the value of the parasitic MOSFET gate capacitance.

8.0 FUTURE PLANS

A SPICE model has been extracted for the delay chain on the Honeywell YCRAT test chip. Test structures have been used to extract parameters for the parasitic and MOSFET circuit elements. SPICE simulation of the delay chain has been performed for three die locations. The modeled and measured data were within 1.5 percent on two die locations and within 5.0 percent on the third. Changes to the test structure and delay chain measurement procedures were incorporated in an attempt to improve predictive capability of the SPICE delay chain model.

Near-term future plans for the Test Structure to Microcircuit Correlation Program include:

1) Verification of the new test structure and delay chain measurement procedures,
2) Perform the pre- and postirradiation measurement procedures for all the die on a single wafer,
3) Compare the measured and modeled delays from the delay chain for all die locations on the wafer and determine the SPICE model predictive capability, and
4) Extract a SPICE model for a read access path on the 2k x 8 SRAM on the YCRAT test chip.

Changes to the delay chain and measurement software have been completed by SNL. These changes included: transition voltages for the HP82000 delay chain measurements, addition of the polysilicon crossbridge measurement, and the MOSFET test structures used in the ΔL and ΔW calculations. The number of test structures used to determine parameters for the delay chain and SRAM have been reduced.

After verification of the changes to the measurement procedures which will be performed jointly by MRC and SNL, the SPICE model predictive capability (model validation) will be checked for all die on a single wafer. First, preirradiation measurements on test structures will be performed to extract SPICE parameters which

are not affected by radiation. Second, MOSFET test structures will be step stress irradiated on the ARACOR to extract postirradiation model parameters for n and p-channel MOSFETs biased on and off during irradiation. Third, the delay chain will be step stress irradiated on the ARACOR. All data will be transferred to MRC for analysis. MRC will produce delay chain SPICE model predictions for each die on the wafer using test structure data taken on the same die. Finally, the predictive capability of the SPICE model will be determined using a statistical Type I and Type II error analysis.

Concurrently with the delay chain work, procedures for extracting a SPICE model for a read access path on the SRAM will be developed. A SPICE model for the entire SRAM will not be extracted due to the large number of circuit elements. The read access path will include switching of the address path and the transfer of the bit information to the output buffers. To correctly model the read access time, all parasitic circuit elements in the read access path must be included. All parasitics in a fan-out for a given MOSFET need to be included even if only one path in the fan-out is contained in the actual signal path. Once the software procedures for extracting a read access path through the SRAM are developed, these procedures can be applied to the extraction of a critical path for any circuit and technology.

The SRAMs on each die location will not be irradiated during the model validation of the delay chain. Once a SPICE model for the read access path can be extracted, parameters for the circuit elements in the SRAM model can be extracted from the same test structure data used for the delay chain. A similar approach as used for the delay chain will be applied to validate and analyze the SPICE SRAM model.

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